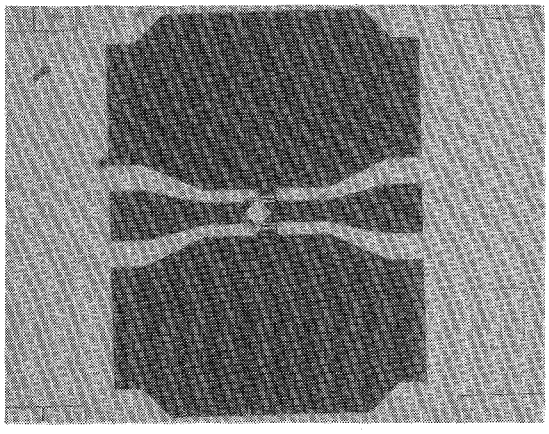

Fig. 4. A photograph of the FET structure in the coplanar waveguide environment.

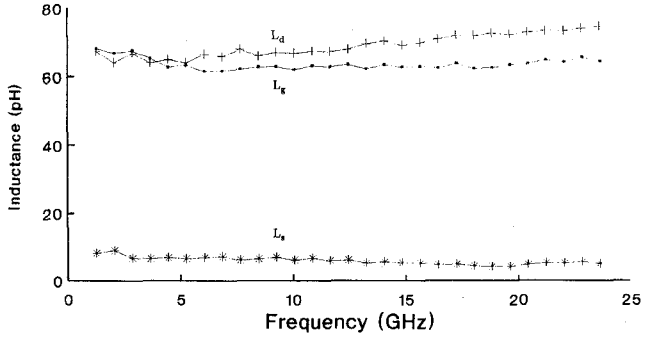

Fig. 5. Variation of the parasitic inductances with frequency.

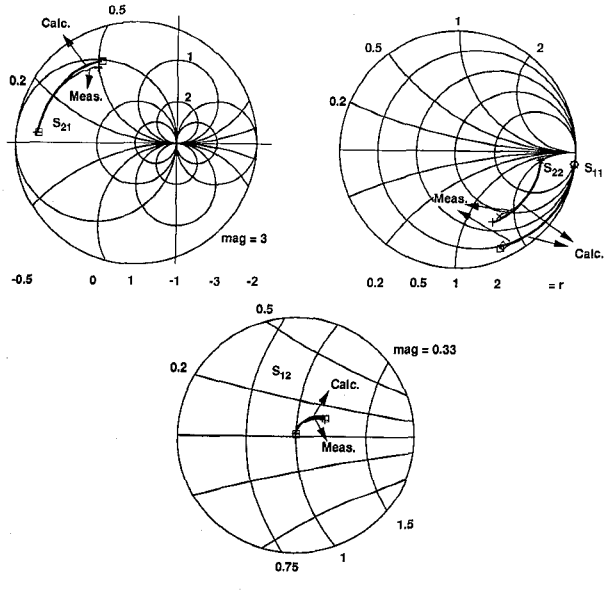

Fig. 6. Comparison of the measured and calculated S-parameters in the frequency range from 1.6 to 22.4 GHz. The calculations are based on the equivalent circuit element values extracted at 10.43 GHz.

The above technique and the equations given in [2] were used to calculate the small-signal equivalent circuit parameters of a pseudomorphic MODFET. The values of measured S-parameters under "active" ("hot") bias condition, and the variation of circuit elements with frequency are shown in Table I. Except for R_i and τ, there is little variation with frequency. Extraction of R_i is difficult since it appears in series with the capacitor C_{gs}. The reactance of C_{gs}, at the frequencies of interest, could be two orders of magnitude larger than the resistance R_i. The value of τ is also affected by the variations in R_i. In order to further investigate the influence of R_i on τ, the value of R_i was set to zero $R_i = 0.0$. The values of τ thus obtained ranged from 0.30–0.43 picoseconds for all the frequencies of Table I, except the first four which varied between 0.12 to 0.70 picoseconds. The polar plots of Fig. 6 show the measured S-parameters and those calculated based on the circuit element values of Table I at 10.43 GHz. Good agreement between the measured and calculated S-parameters is observed over the whole frequency range especially at lower frequencies.

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Microstrip Quarter-Wave High Voltage DC Block

Thomas E. Koscica

***Abstract*— A microstrip high voltage dc block is presented. Silicon rubber is used to insulate a quarter-wave coupler and the resulting effective dielectric constant and impedance are discussed. DC isolation up to 4500 V is achieved.**

I. Introduction

The need for dc blocks that can handle over several hundred volts can be grouped into two areas: First, the biasing of high voltage devices such as vacuum tubes, IMPATT devices, and electrooptic phase shifters. Second, the protection enhancement of bias tees and microwave equipment incorporating them.

Standard coupled line bias gaps, [1]–[4], have well developed microwave models with good performance for voltage supplies less than 200 V, depending on humidity. Above this bias level, attention must be given to voltage breakdown of either air or the dielectric of a lumped element capacitor where used.

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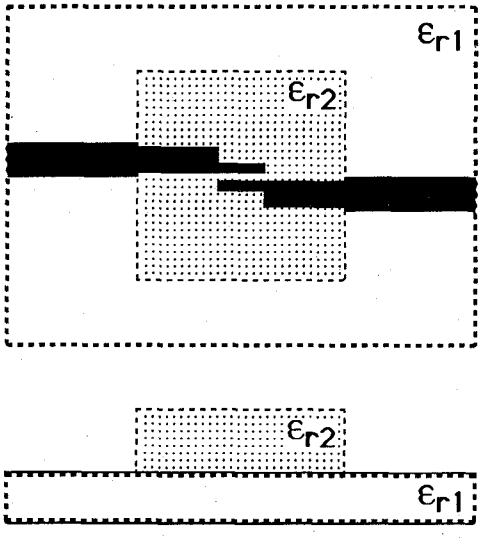

Fig. 1. Top and side views of high voltage bias gap showing high voltage insulator dielectric.

Recently a novel ground plane dc block for microstrip was introduced, [5], and subsequently extended, [6], to withstand voltages as high as 4 kV. Two issues limit its acceptance in high voltage applications: First, the present dependence on empirical data until a suitable modeling method is developed. Second, the long gap across which high voltage is applied; any processing flaw along this gap length results in reduced voltage breakdown protection.

The high voltage dc block discussed in this paper is shown in Fig. 1. It is based upon quarter wave coupled lines with the addition of a layer of silicon rubber to provide protection against voltage breakdown across the gap. As compared with the published microstrip high voltage dc block, [6], the design discussed in this paper features reduced complexity, need for single side processing only, increased breakdown voltage, increased reliability, and availability of a suitable modeling method. It is straightforward to extend the design principles to other substrates, insulating coatings, frequencies, and multicoupled line filters.

II. Analysis

The high voltage bias gap of Fig. 1 is similar in operation to a standard quarter wave dc block for microstrip. The microstrip dc block with dielectric overlay must be analyzed to determine how the silicon dielectric affects the even and odd mode impedances of the coupled lines. In order to achieve good bandwidth with low standing wave ratio (SWR), the gap separation, s, and coupled line width, w, need to be adjusted. Additionally, the overlay material changes the effective dielectric constant along the coupled lines. By using this effective dielectric constant, the length of the coupled line section can be adjusted in order to get the required center frequency.

First consider the section of transmission line immediately next to the coupled line region. This section is coated in order to insure that the coupled lines have a guard region of silicon rubber.

In order to get the effective dielectric constant of this overlay microstrip region, which is needed for appropriate transmission line impedance designs, the variational technique combined with the transverse transmission line method, [7], is used. This method generates values for $C_{\epsilon r}$, the capacitance per unit length with the substrate and overlay dielectrics present as shown in Fig. 2, and C_{air}, the capacitance per unit length for both dielectrics replaced by air. In terms of these two values, the effective dielectric constant for the

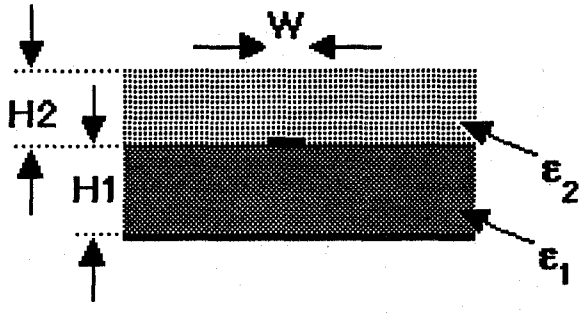

Fig. 2. Cross section of overlay microstrip.

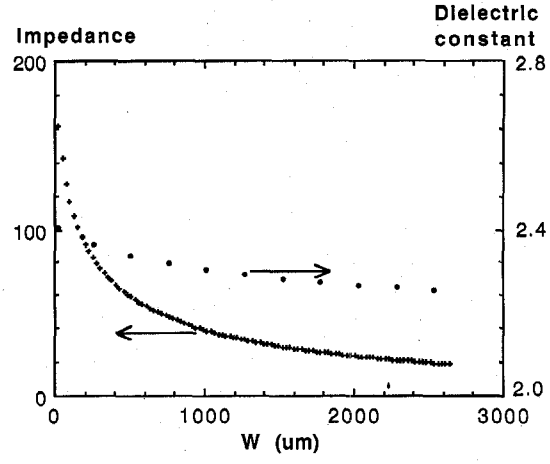

Fig. 3. Impedance and ϵ_{eff} data for overlay microstrip with $\epsilon_{r1} = 2.2, \epsilon_{r2} = 2.7, H1 = 254\mu\text{m}, H2 = 2540\mu\text{m}$.

overlay microstrip is [8]:

$$\epsilon_{\text{eff}} = \frac{C_{\epsilon r}}{C_{\text{air}}}$$

Results for various metallization widths are shown in Fig. 3. One can get the impedance of the overlay microstrip line by using the following expression derived from [8]:

$$Z = \frac{1}{c_o \sqrt{\epsilon_{\text{eff}}} C_{\text{air}}}$$

where the value used for C_{air} is obtained from standard microstrip equations, [9], [10], using $\epsilon_r = 1$.

The next step in analyzing the high voltage gap is to determine the dimensions of the coupled lines.

A criteria for microwave design is that given the required SWR and bandwidth, the physical dimensions are determined. By using [12], SWR and bandwidth are mathematically relted to Z_{oe} and Z_{oo}, the required even and odd mode impedances values for the coupled lines. From [12]:

$$Z_{oe} = \sqrt{S}\left[1 + \sqrt{1 + \frac{1 + \sqrt{1 + \Omega_c^2}}{\Omega_c^2}\left(1 - \frac{1}{S}\right)}\right]$$

$$Z_{oo} = \sqrt{S}\left[-1 + \sqrt{1 + \frac{1 + \sqrt{1 + \Omega_c^2}}{\Omega_c^2}\left(1 - \frac{1}{S}\right)}\right]$$

where S is the standing wave ratio and Ω_c is a normalized bandwidth as described in [12].

To relate the even and odd mode impedances to physical dimensions, the variational technique combined with the transverse transmission line method, [7], is used to obtain values for $C_{\epsilon r(\text{even})}$ and $C_{\epsilon r(\text{odd})}$, the even and odd mode capacitances per unit length of

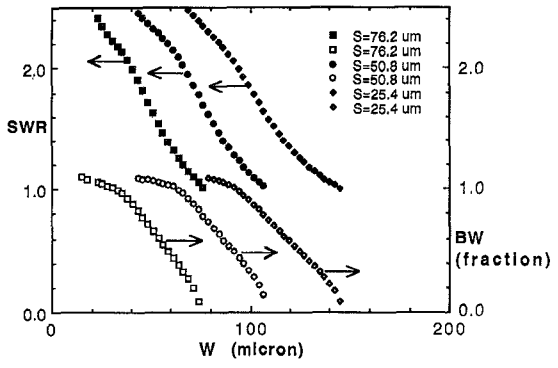

Fig. 4. Calculated SWR and bandwidth as functions of s and w.

the coupled lines with the dielectric overlay present, and $C_{\text{air(odd)}}$ and $C_{\text{air(even)}}$, the capacitance per unit length with all dielectric replaced by air. Then the effective dielectric constants for the coupled lines are [8]:

$$\epsilon_{\text{eff(even)}} = \frac{C_{\epsilon r\text{(even)}}}{C_{\text{air(even)}}}$$

$$\epsilon_{\text{eff(odd)}} = \frac{C_{\epsilon r\text{(odd)}}}{C_{\text{air(odd)}}}$$

One can get the impedance on the etched dielectric microstrip line by using the following expression which can be easily derived from [8]:

$$Z_{oe} = \frac{1}{c_o\sqrt{\epsilon_{\text{eff(even)}}}C_{\text{air(even)}}}$$

$$Z_{oo} = \frac{1}{c_o\sqrt{\epsilon_{\text{eff(odd)}}}C_{\text{air(odd)}}}$$

The effective dielectric constant for the coupled lines becomes:

$$\epsilon_{\text{eff}} = \sqrt{\epsilon_{\text{eff(even)}}\epsilon_{\text{eff(odd)}}}$$

Computer calculations based on the above method result in obtaining SWR and bandwidth as functions of the gap width, s, and the coupled line width, w. Results are presented in Fig. 4.

The length of the coupled lines is slightly less than $\lambda g/4$ where λg is $\lambda o/\sqrt{\epsilon_{\text{eff}}}$ and λo is the wavelength in air at the center of the passband. The slight reduction is due to end effects since square discontinuities are used without compensation, [11].

III. Experimental

Several circuits were constructed resulting in SWR and bandwidth values only slightly worse than predicted. Modeling for finite thickness conductors, as well as the use of a compensation curve similar to reference [11], are possible improvements. Both of these effects are not included in the basic analysis, [12]. Of interest here is that a duroid based circuit with $s = 50\mu$m, $w = 60\mu$m, gave a voltage breakdown over 4500 V. When breakdown does occur, it is often at one of the open ends of the coupled lines. This occurs because of the increased dc electric field which occurs at these ends. Rounding the open ends of the coupled lines reduces the field stress at these points and suppresses this failure mode. By making the gap width larger, one can get increased voltage breakdown protection at a tradeoff of poorer SWR and bandwidth characteristics.

IV. Conclusions

The three constraints on high voltage bias gap design using quarter wave coupled lines are SWR, bandwidth, and voltage breakdown. Since for a given substrate thickness only the gap width and coupled line width can be varied, the problem is over constrained. It happens that typical gap separations used for achieving a required SWR and bandwidth result in sufficiently high voltage dc blocks; the over constraint is then not a problem of concern.

Breakdown voltages over 4500 V are routinely obtained by the method described in this paper. This represents an increased voltage protection capability in a circuit that has a form which can be modeled. These principles can easily be extended to many element coupled line filters to achieve any standard passband characteristic with improved high voltage protection.

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